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Practical Project: Design and construction of a high quality 100MHz bandpass filter

The editors of VHF Communications and UKW Berichte recently issued a call for readers to describe successfully implemented projects and thus to give a new impetus to the activities of DIYers. Here is just such a project that required "intermediate development" at short notice. It did take longer than was expected to develop the circuit and to make sure that the targets were achieved.

1. Range of application

New projects are continually required for practical laboratory work. Various kinds of receivers or converters can be assembled from a set of microwave parts, some of these will be available and some will have to be designed and built, such as low noise amplifiers, mixers, stripline filters, VCOs etc.

A standard commercial car radio with synthesiser tuning and built in final stages (2 x 12 Watts) can be used as a 100MHz low frequency amplifier to reproduce FM or PSK signals, and for audio demonstrations to large groups of people.

The car radio was selected because such radios have high sensitivity and good screening built in as standard features, and frequencies can also be easily adjusted or saved through a menu driven operation.

This bandpass filter can be connected between the intermediate frequency output of a microwave converter and the antenna input of the radio to ensure that in practice only signals converted to 100MHz are audible even if it is the image frequency.

2. Specifications

The following specifications were laid down for the development of the bandpass filter:

- System impedance: $Z = 50\Omega$
- Degree of filtration: $n = 5$
- Centre frequency f_0: 100MHz
- 3dB bandwidth: b = 5MHz
- S21 Ripple in transmission range: 0.3dB
- Transmission loss in pass band: < 10dB
- Edge steepness: at 90MHz or 120MHz the attenuation should have risen to approximately 70dB with respect to the transmission range
- Filter attenuation in stop band in

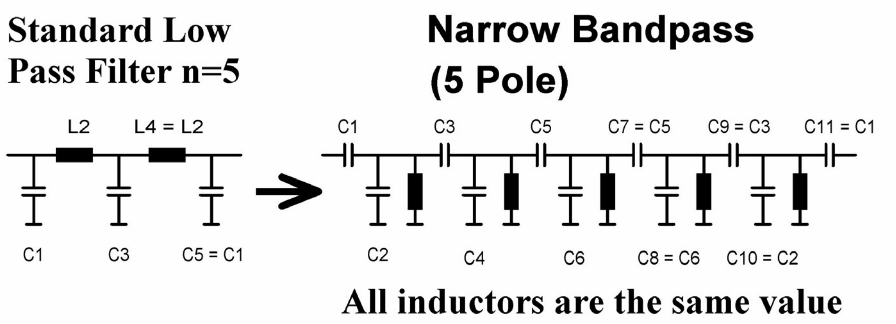


Fig 1: The standard low pass filter is transformed to the narrow bandpass filter with series capacitors and shut inductors.

frequency range from 0 to 1GHz min. 70dB

- Filter type: Chebyshev Narrow Bandpass
- Mechanical: Printed circuit board, coated with 35µm copper on both sides, made from Rogers material R04003 with a thickness of 25 MIL = 0.813mm
- Board dimensions 30 x 130mm. Incorporated into a milled aluminium housing with SMA sockets as input and output
- Distance between board and cover, 13mm.

Following some test simulations, the so-called "Narrow Bandpass" was selected as the filter type, with n = 5, which can achieve very small bandwidths. It is created from the familiar, standard, low pass filter by suitable transformation work and is characterised by the fact that the inductances are the same value in all the resonant circuits.

As a result of experience, L = 100nH was selected (for with reactive impedances exceeding 80 to 100 Ohms at 100MHz for coils or capacitors, problems rapidly arise with the broadband nature of the filter properties). This only works correctly if components of the highest possible quality are used.

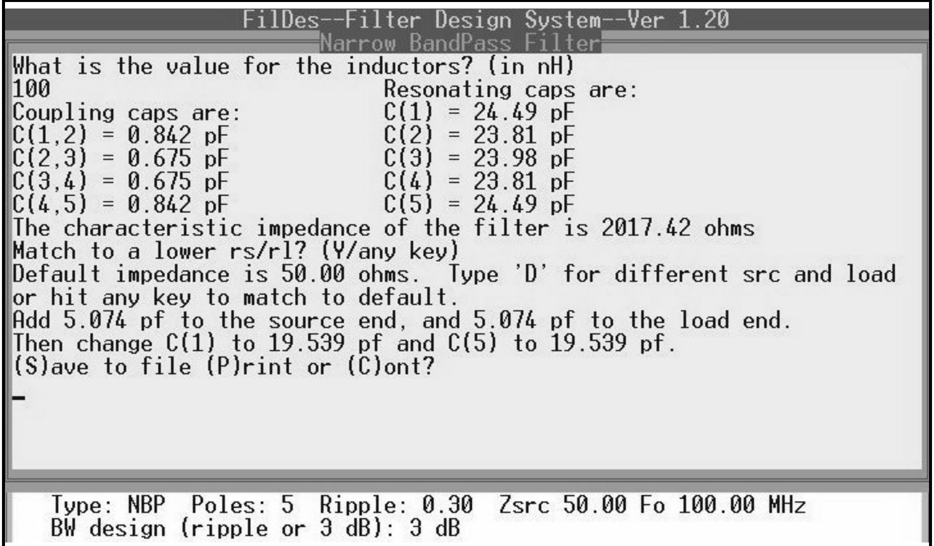
This also applies to the circuit board, hard paper or FR4 material should not be used. Only genuine microwave materials are permissible, made from Teflon, ceramics or modern materials such as Rogers R04003 which has the combination of excellent mechanical and electrical characteristics which are not far below those of Teflon, even at 10GHz.

This type of filter is essentially high impedance, so it must be matched to the 50Ω source or load by means of an input or output capacitor.

The circuit diagram is shown in Fig. 1. The actual filter calculations are carried out using the free filter CAD program "fds" available from the Internet.

3. Circuit diagram of filter

Entering the design information into the input mask of the filter program (fds), we obtain a picture like Fig. 2. You should take the trouble to draw the associated circuit immediately, because this is actually where we start to think about the practical implementation.



```
FilDes--Filter Design System--Ver 1.20
Narrow BandPass Filter
What is the value for the inductors? (in nH)
100                          Resonating caps are:
Coupling caps are:           C(1) = 24.49 pF
C(1,2) = 0.842 pF            C(2) = 23.81 pF
C(2,3) = 0.675 pF            C(3) = 23.98 pF
C(3,4) = 0.675 pF            C(4) = 23.81 pF
C(4,5) = 0.842 pF            C(5) = 24.49 pF
The characteristic impedance of the filter is 2017.42 ohms
Match to a lower rs/rl? (Y/any key)
Default impedance is 50.00 ohms.  Type 'D' for different src and load
or hit any key to match to default.
Add 5.074 pf to the source end, and 5.074 pf to the load end.
Then change C(1) to 19.539 pf and C(5) to 19.539 pf.
(S)ave to file (P)rint or (C)ont?
_

   Type: NBP  Poles: 5  Ripple: 0.30  Zsrc 50.00 Fo 100.00 MHz
   BW design (ripple or 3 dB): 3 dB
```

Fig 2: The results produced by the filter design program "fds".

As already mentioned we will need coils of extremely high quality and stability, so here we use industrially manufactured helical components, e.g. from Neosid, with L = 100nH and a basic Q of 130.

The circuit capacitors, like the input and output capacitors, are a combination of two or three SMD size 0805 standard values made from "NP0" material or better. The tiny coupling capacitors are under 1pF and must be accurate so only printed inter-digital capacitors can be considered. Fig. 3 shows the complete circuit design.

As a check, two simulations of the filter characteristics for the ideal case were carried out using PUFF. Fig. 4 shows the frequency range from 90 to 110MHz, it is easy to recognise that the requirement for "at least 70dB filter attenuation at 90MHz" is adequately met. Fig. 5 shows the permissible Chebyshev ripple of 0.3dB in the pass band and confirms the efficiency of the free filter program used.

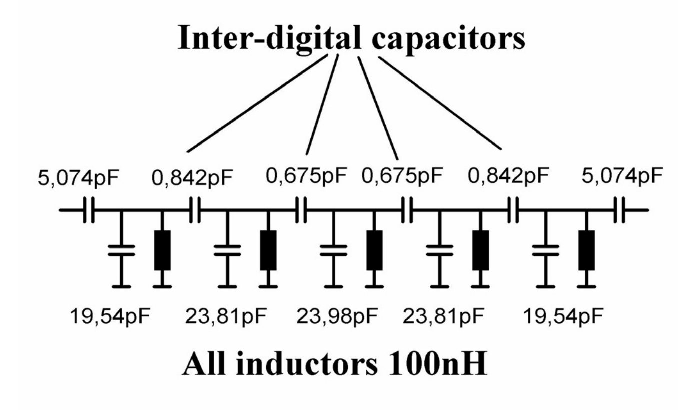


Fig 3: The completed circuit showing the capacitors that must be constructed as inter-digital devices.

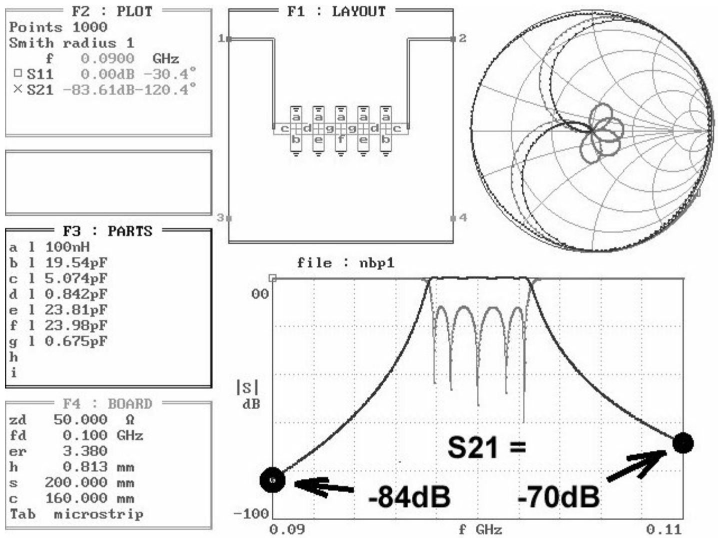


Fig 4: PUFF simulation showing adequate attenuation at 90 and 120MHz.

4. Realisation of the inter-digital coupling capacitors

The values required for the coupling capacitors are very low and lie between 0.5 and 0.9pF, but must be produced with a high degree of precision. For this reason, discrete solutions are excluded, and we are left with a "printed format".

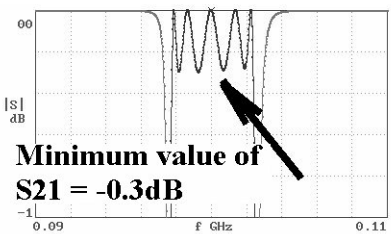


Fig 5: Chebyshev ripple in the pass band.

The design of such capacitors, using nomograms, has already been described in VHF Communications articles. [1] [2].

However, when the first attempts were made to assemble the printed circuit on the board, it became clear that the divergences of 10% to 15% between theory and practise arising using these procedures can not be tolerated and another solution is required. Fortunately, the free student version of APLAC allows for the simulation of an individual capacitor of this type with really high precision, although it then refuses to examine the complete filter circuit saying "Memory restricted in this version....".

We therefore propose the following path:

- The two inter-digital capacitors required (0.675pF and 0.842pF) are individually developed and optimised one after the other. In addition, an S parameter file is generated for each capacitor that can be entered into the PUFF simulation.
- The complete filter circuit is first simulated using PUFF and then

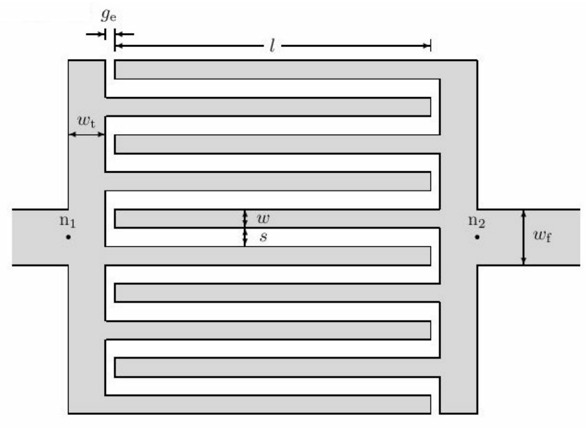


Fig 6: APLAC model for an inter-digital capacitor showing the relevant dimensions.

manually optimised (the inter-digital capacitors not only affect coupling but also add extra inherent capacitance to the circuit capacitors, the latter must be correspondingly reduced).

- Only now is the coil Q taken from the data sheet also inserted into the circuit as a loss resistance for any inductance and thus simulates the transmission curve to be expected from the structure of the printed circuit board.

We began with the design of the small capacitor of 0.675pF. The first step, according to the start of the APLAC program, is to open a new file and then right click on the empty screen. Under "Basics", we find the components "Port" and "Ground", each one is needed twice (but in the student version they have to be called up individually one after the other). The inter-digital capacitor can be inserted by right clicking on mouse / microwave / microstrip / Micap. Following positioning of these five components, double click on the left hand mouse button on a free space, which allows a roll of wire to come out of the cursor and the circuit can be wired up (see also the APLAC presentation in [3]).

The S parameter file for the simulated capacitor is not generated until you have clicked on the output port and, under "Attributes", entered the line

STORE C0675.s2p GHZ MA

The two system resistance ports have already been automatically selected at 50Ω, as the entry "50" is automatically posted. However, to make things clearer, you should always make all attributes visible. Now the crucial question arises: how are the technical details of an inter-digital capacitor programmed?

Fig. 6 can help us here, since it originates from the corresponding manual (RF Components / Microstrip Parts / Micap) and tells us what APLAC needs for correct simulation, where:

- W = Finger width
- L = Finger length
- N = Number of fingers
- S = Finger interval
- Ge = Gap at end
- WT = Width of connecting line for individual fingers on each side, which is indicated as Transmission Line.
- WF = Width of microstrip supply line leading to capacitor connections

0.25mm was selected for the finger widths and the various intervals. Firstly, this can be controlled satisfactorily by the board manufacturer, and secondly

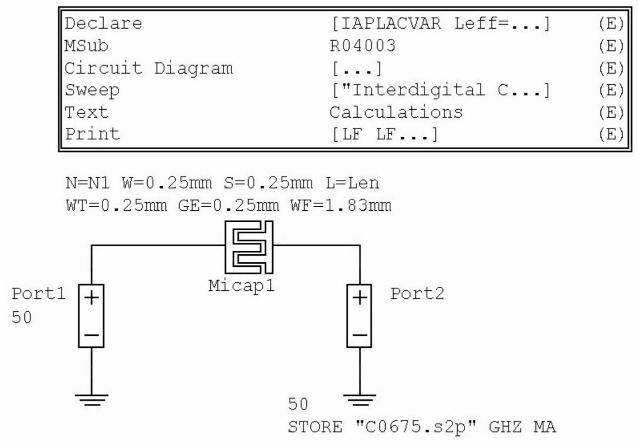


Fig 7: The completed simulation of an inter-digital capacitor using APLAC.

this value is not so high that it brings the desired coupling capacity down too far.

The selection of six fingers was based on the older designs already mentioned [1], [2], and the start value for the finger lengths was likewise taken from them and subsequently optimised. These values must now be correctly transferred into the attribute field of the capacitor (after double clicking on the symbol) In Fig. 7 all the moves discussed can be seen. Just make sure that an additional variable, "N1", has been introduced for the number N, and that a new variable, "Len", has likewise been introduced for the finger length. This is not absolutely necessary, but it makes things clearer for outputting the calculated values later. Moreover, it is now high time this project was saved under a suitable name.

In addition, the "Object Box List" was also mixed in. It keeps a record of the necessary simulation files and can always be called up onto the screen using "Presentation / Show Object Box List". The entry "Isweep" (which can not be used here!) is deleted.

Five new files have to be added to existing "Circuit File". These are described in detail below. Please note that the sequence of the following files in the Object Box List must be adhered to...

The "Declare" file

In this file, all "Initialised APLAC variables" (IAPLAC- VAR) required later are declared. They must always have a start value of some sort. In the simplest case, just enter a "1". We then have:

IAPLACVAR Leff=1.0
IAPLACVAR Cg=1.0
IAPLACVAR Cm=1.0
IAPLACVAR Cgtot=1.0
IAPLACVAR Cmtot=1.0
IAPLACVAR Len=7.30mm
IAPLACVAR N1=6

Comments:

Leff - represents the actual effective finger length, calculated by the program.

Cg - expresses the grounded capacitance per unit length, i.e. the additional relative inherent capacitance per unit length arising. It will detune the resonant circuit to the left and right of the capacitor.

Cm - corresponds to the coupling capacity desired, though once again expressed per unit length.

Cgtot - is the actual effective inherent capacitance for each individual capacitor connection, by which the associated capacitor must be reduced. It is calculated as the product of Cg and the effective length, Leff.

Table 1: Contents of Sweep file.

"Interdigital Capacitor 0.675pF"						
LOOP	1001	FREQ	LIN	0.000001GHz		3GHz
WINDOW=0		Y	""	"dB"	-40	0
SHOW W=0			Y	MagdB(S(1,1))		
		+Y	MagdB(S(2,1))			

Cmtot - is the true objective: the actual coupling capacitance, calculated as the product of Cm and Leff

Len represents the finger length verifiable in the layout

N1 - is the number of fingers used.

The "Msub" file

All the data concerning the board material (Rogers R04003) and the circuit board are contained in this file. The following entries are needed:

ER=3.38

H=0.813mm

T=0.035mm

RHO=0.75

RGH=2um

TAND=0.0005

COVER=13mm

LEVEL=2

The following details are included, in this order:

Relative permittivity: 3.38
Board thickness: 0.813 mm
Copper coating: 35 µm
Specific resistance of copper in comparison with gold: 0.75
Surface roughness: 2µm
Board material dielectric loss factor: 0.005 where f = 100MHz
Distance between board and cover: 13 mm
LEVEL = 2 means simulation must be extremely precise, regardless of the amount of calculation

The "Circuit" file

It is automatically set up when the wiring diagram is drawn and no additional entries are required.

The "Sweep" file

This is not only used to generate the S parameter file for the desired capacitor, but also allows S11 and S21 to be represented in the frequency range from 1kHz to 3GHz. A start value of 1kHz is used because AppCad 3.0 gives an error message if the frequency in an S parameter file begins with zero.

The "Sweep" file required is shown in Table 1.

Significance of individual lines of "Sweep" file:

- 1st line: Designation of simulation project, included in desired printouts
- 2nd line: Simulate 1001 points in frequency range from 1kHz to 3GHz and divide this range up linearly.
- 3rd line: Provide diagram for outputting results with vertical axis divided up from 40dB to zero dB.
- 4th line: It must always be empty, must NEVER be forgotten and separates the simulation section from the display section
- 5th line : Display magnitude cycle of S11 in zero window
- 6th line: Display magnitude cycle of S21 in same window.

The "Text" file

This is used in calculation and saved separately as a public declared variable, and subsequently determines the precise capacitor data (see entries and comments in "Declare" file):

Call Leff=Ref(Micap1,L)

Table 2: Contents of Print file.

```
LF LF
S "Calculation of an Interdigital Capacitor of 0.675pf"
LF LF
S "Number of Fingers = "REAL N1
LF
S "Length of a finger = "REAL Len
LF
S "Total grounded capacitance on every side = "REAL Cgtot
LF
S "Total coupling capacitance = "REAL Cmtot
LF
```

```
Call Cg=Ref(Micap1,C1)
Call Cm=Ref(Micap1,C)
Call Cgtot=Cg*Leff
Call Cmtot=Cm*Leff
```

The"Print" file

It provides for the outputting of the calculated parallel and coupling capacities on a page of their own. To make things clearer, "LF" stands for line feed. And "S" identifies a string. This is the associated explanatory text (Table 2).

If this work is correctly done (and the new files are listed in the specified order), the simulation can be started using <Control + S>.

After the necessary calculation time, something appears on the screen. But only the printout is important (Fig. 8), whilst the representation of the S parameter is more for information. To make things clearer, it should be explained that the calculated values are always output in the basic units. The entries must therefore be indicated in the following way:

- Number of fingers = 6
- Finger length = 7.30mm
- Total effective inherent capacitance on each side = 535.489 Femtofarads = 0.535pF

```
APLAC 7.51 Thu Dec 26 2002 at 07:50:15
Copyright (c) APLAC Solutions Corporation, Finland, 1998-1999

APLAC 7.51 WARNING: Mlin T less than three skindepths
 (TLine_VCCS2<-Mlin_TLine<-tim2<-Micap1)

Calculation of an Interdigital Capacitor with 0,675pF

Number of Fingers =  6.000
Length of a finger =  7.300m
Total grounded Capacitance on every side =  535.489f
Total coupling capacitance =  675.010f

   End of APLAC 7.51 Thu Dec 26 2002 at 07:50:18 (CPU-time =  2.89 s)
```

Fig 8: The APLAC printout for the 0.675pF inter-digital capacitor.

Table 3: Setup file for PUFF showing important parameters in bold.

\b{oard}	{.puf file for PUFF, version 2.1d}	
d	0	{display: 0 VGA or PUFF chooses, 1 EGA}
o	1	{artwork output format: 0 dot-matrix, 1 Laser Jet, 2 HPGL file}
t	0	{type: 0 for microstrip, 1 for stripline, 2 for Manhatten}
zd	50.000 Ohms	{normalizing impedance. 0<zd}
fd	**0.100GHz**	**{design frequency. 0<fd}**
er	**3.380**	**{dielectric constant. er>0}**
h	**0.813mm**	**{dielectric thickness. h>0)**
s	200.000mm	{circuit-board side length. s>0}
c	160.000mm	{connector separation. c>=0}
r	0.010mm	{circuit resolution, r>0, use Um for micrometers}
a	0.000mm	{artwork width correction.}
mt	**0.035mm**	**{metal thickness, use Um for micrometers.}**
sr	**5.000Um**	**{metal surface roughness, use Um for micrometers.}**
lt	**5E-0004**	**[dielectric loss tangent.}**

- Total coupling capacitance = 675.01 Femtofarads = 0.675pF.

The 0.842pF capacitor is also calculated in this way. In the "Declare" file, the number of fingers is altered to N1 = 8 and the finger length is changed to Len = 6.44mm. And dont forget to double click on the output port on the screen and change the designation of the S parameter file in "C0842.s2p". Now save, under a new name, and then check the sequence of files, carry out a simulation and incorporate the result:

- Number of fingers = 8
- Finger length = 6.44mm
- Total effective inherent capacitance on each side = 601.940 Femtofarad = 0.602pF
- Total coupling capacitance = 842.387 Femtofarad = 0.842pF.

So APLAC has completed its task and can be shut down again.

5. Preparation of circuit with the help of PUFF

Preliminary note on PUFF:

To simplify working with PUFF, we create a new folder for a new project and unzip or copy PUFF2.1 into it. This folder is then given the name of the corresponding development and an Icon with the same name on the Windows screen. You should only work with the better Protected Mode version of PUFF and should therefore set up a path to the puffp.exe file! Right click on your PUFF icon and select the properties. Select the memory tab and use the settings shown as per [4] and [5]. Activate "Auto" under the "Conventional memory" heading in both windows. Under EMS, XMS and DPMI the entry required is 4096 Kilobyte. You can now experiment with PUFF without problems. Once development work has been completed, only the results data are saved, and then the operations folder is deleted again.

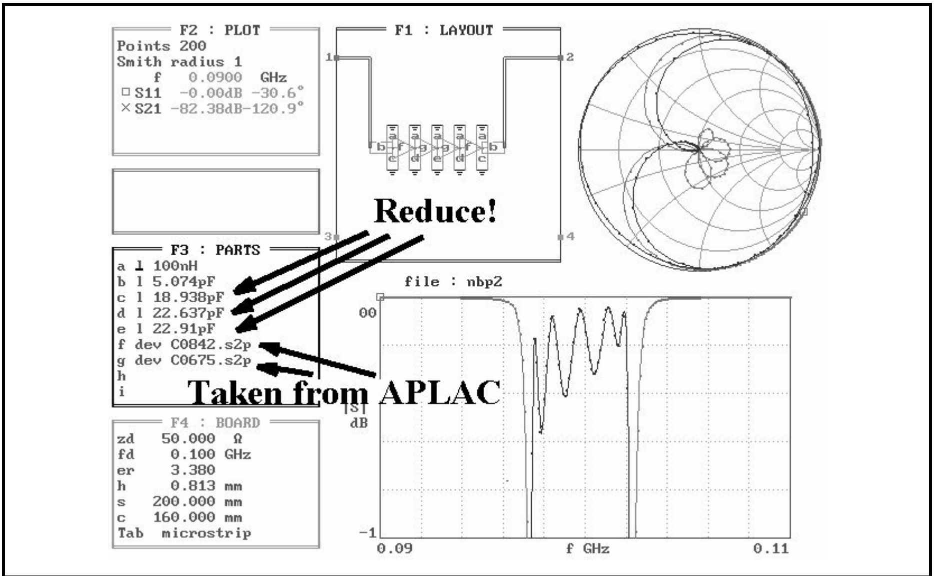


Fig 9: PUFF simulation using inter-digital capacitors showing results that are not ideal.

After that preliminary note, we can get started. Open Windows Explorer and copy the two S parameter files generated by ACLAP (C0675.s2p and C0842.s2p) into this new PUFF folder. Then use the text editor to open the setup.puf file, to enter the correct material and circuit board data.

Table 3 lists the data from the file for the Rogers R04003 circuit board used (the important points are in bold type!).

Once this is complete, start PUFF and enter one component after another in list F3. However, the entire circuit must be modified compared with Fig. 3 and Fig. 4, at the following points:

Instead of the discrete coupling capacitors with 0.675pF or 0.842pF, the two S parameter files generated by APLAC, C0675.s2p and C0842.s2p, are now used. This happens in F3 with the two lines:

device C0675.s2p
device C0842.s2p

In addition, in all five resonant circuits the circuit capacitors must be reduced by the additional inherent capacitances introduced by the adjacent inter-digital structures. This produces the following changes:

- First and fifth circuits:
  Ccircuit = 19.540pF 0.602pF = 18.938pF
- Second and fourth circuit:
  Ccircuit = 23.810pF 0.602pF 0.535pF = 22.637pF
- Middle circuit:
  Ccircuit = 23.980pF 0.535pF 0.535pF = 22.91pF

If we now repeat the simulation as per Fig. 4 with this circuit changed in this way, the result seems rather a long way from the desired ideal (Fig. 9). Fortunately, the solution is relatively simple, since the reason for this situation should be sought in the (simple!) relationships between the frequencies and the inter-digital capacitance values! So you keep making careful corrections to the values of the resonant circuit capacitors until you have achieved the best compromise. Fig. 10 shows this objective and the

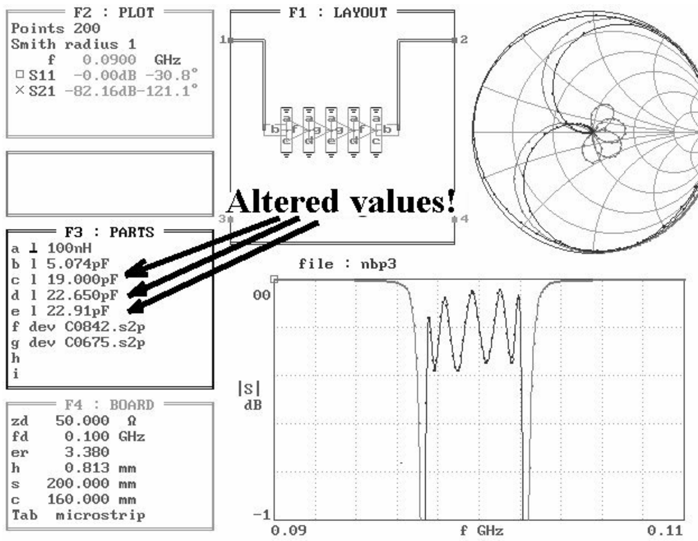


Fig 10: PUFF simulation using inter-digital capacitors showing results after adjusting the capacitor values.

capacitor modifications required for it.

Things don't get interesting until you bring the actual coil losses present into the simulation. With the Neosid helical filters used, the data sheet specifies a basic Q of Q = 130 for the frequency f = 100MHz. However, if you rotate the core inward during adjustmets in order to reduce the inductance, then this quality is reduced! We are actually dealing with brass cores, into which eddy currents are induced via the coils magnetic field, thus reducing the inductance. But this is equivalent to an increase in losses and it is more advantageous to work with a quality of only Q = 100. If we consider these losses as a series resistor for each coil, then we must set 0.63Ω on each side. Fig. 11 shows the effects of these losses. They cause the transmission loss to increase to approximately 7.3dB, whilst the stop band remains practically unchanged.

It becomes interesting later on to compare the measured results with this prediction, for so far, very optimistically, we have assumed that all circuit capacitors are ideal and loss free and we must therefore undoubtedly count on another slight deterioration.

6. Practical construction of the bandpass filter

The board dimensions are defined by the home made milled aluminium housing, with a screwed on screening cover, used by the author. These dimensions are used for all microwave circuits and, on grounds of rationalisation, they now come in only the two board sizes, 30mm x 50mm and 30mm x 130mm. The four fixing screws are then arranged in a grid, 24mm x 44mm or 24mm x 124mm.

If you take a closer look at the bandpass filter circuit board (Fig. 12), you will very quickly recognise the principle used, which is a tried and trusted one for microwave circuits:

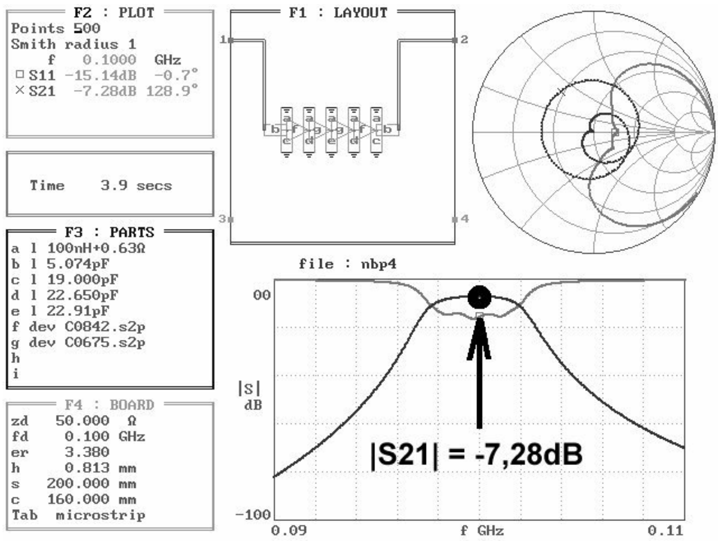


Fig 11: PUFF simulation showing the effect of losses.

The underside of the circuit board is a continuous earthing area. The two SMD coupling capacitors are inserted at the input and output in the continuous 50Ω microstrip line, which has a width of 1.83mm, on the top face. In addition, this line is interrupted by the four inter-digital capacitors required. The five insulated earthing areas, with numerous feed through links, are designed for the five resonant circuits. Do not use any other earthing areas for frequencies from 100MHz upwards, since these through hole plated islands ensure low inherent instability and satisfactory broadband behaviour!

The helical filters do pose one small problem due to their overall height, which with the connecting feet are approximately 15mm, and thus exceeds the clearance height of 13mm between the circuit board and the cover. This problem is solved by flush mounting with the silver plated housing soldered directly to the associated earth islands.

The circuit diagram and the components required can be seen in Fig. 13, whilst Fig. 14 shows the final structure.

If you add up the capacitances in each individual circuit and compare them with the values calculated above and then add

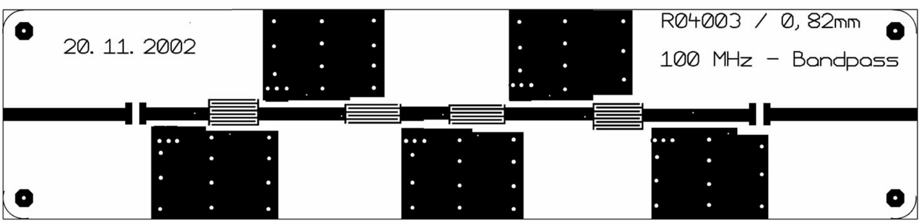


Fig 12: Printed circuit board layout for the 100MHz bandpass filter.

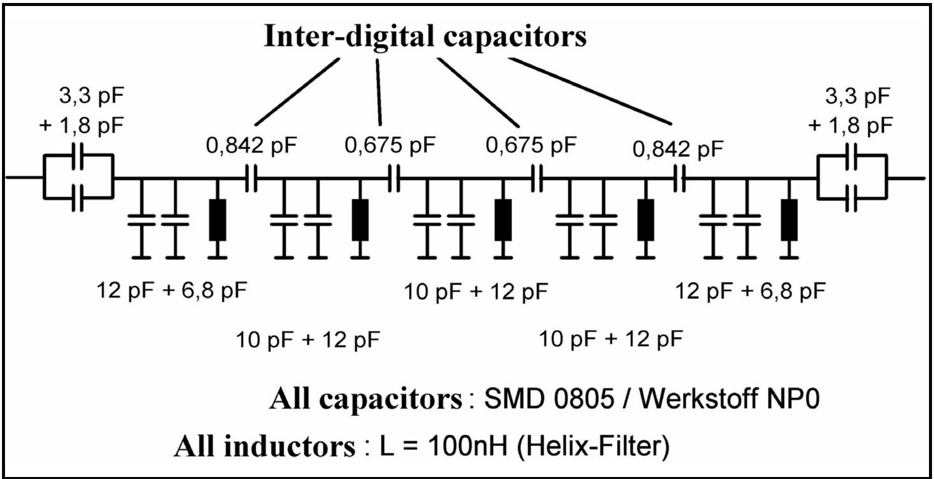


Fig 13: Final circuit diagram for the 100MHz bandpass filter.

in the capacitance of the continuous stripline (the circuit board data selected gives an inherent capacitance of approximately 0/5pF for a line length of 5mm), you come to the conclusion that the soldered component values are too high!. This is true, but when the core is fully rotated out the helical filters have a maximum inductance of 100nH, which can be reduced right down to 93nH when the core is rotated in (see above!). Thus it is preferable to add a little extra to the capacitance and tune the filter correctly. The following measurements indicate that these observations are correct.

One problem remains: after the filter is built how do you get at the inductor cores? One solution would be suitably positioned tapped holes in the housing, which are closed using grub screws. But a second method works better on this filter, with minimal stray fields. Use two small copper plates as carriers for the two SMA sockets at the input and output. The central conductors of the sockets are soldered to the associated microstrip lines and the plate squares are simply screwed to the circuit board. Fig. 15 shows this arrangement. Now the circuit board can be connected to the network analyser, measured and correctly tuned.

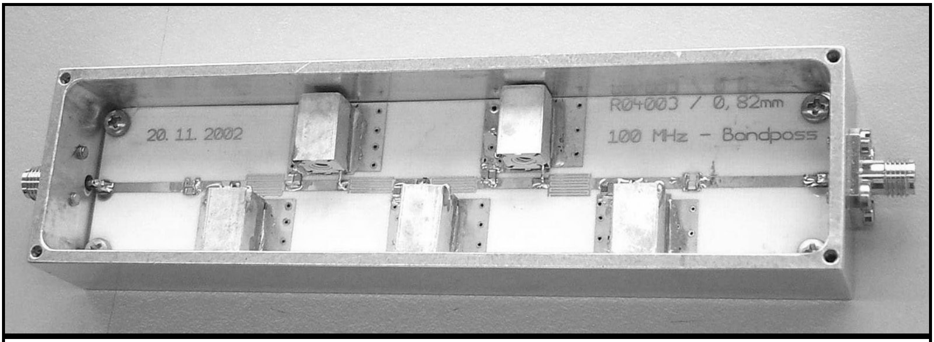


Fig 14: The completed 100MHz bandpass filter in its aluminium housing.

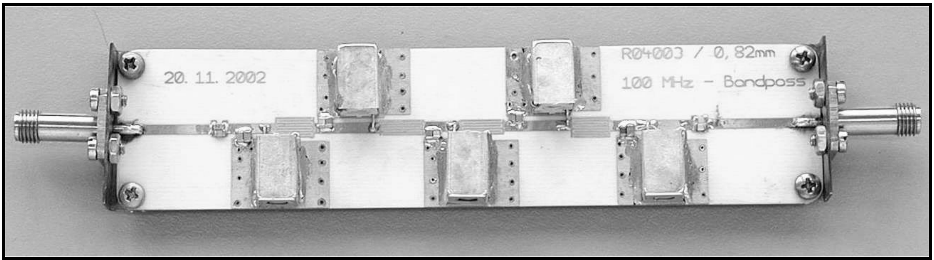


Fig 15: The bandpass filter with SMA connectors fitted to copper plates.

A subsequent measurement check following incorporation into the screening housing, with the cover screwed on, shows that the transmission curve is not noticeably altered as a result.

Incidentally: this method is also extremely useful for rapid, basic functional testing of all microwave circuits in the range up to 10GHz. When equipment is in a housing the first thing you are usually struggling against is the fact that the layout acts as a waveguide or a cavity resonator, with its natural resonances and other effects. It usually needs a bit of effort, e. g. using conducting foamed material glued to the inside of the cover or additional dividing walls, to get control of these “bad habits”.

7. Measurement results

Fig. 16 shows the transmission curve in the frequency range from 90 to 110MHz, so that we can make a direct comparison with the simulation as per Fig. 11. Naturally, there are difficulties with the rise in the transmission loss to 10dB (as we feared). If we carry out a few more specimen simulations with varying loss resistance values, then this gives us a series resistance of 0.88Ω for each coil,

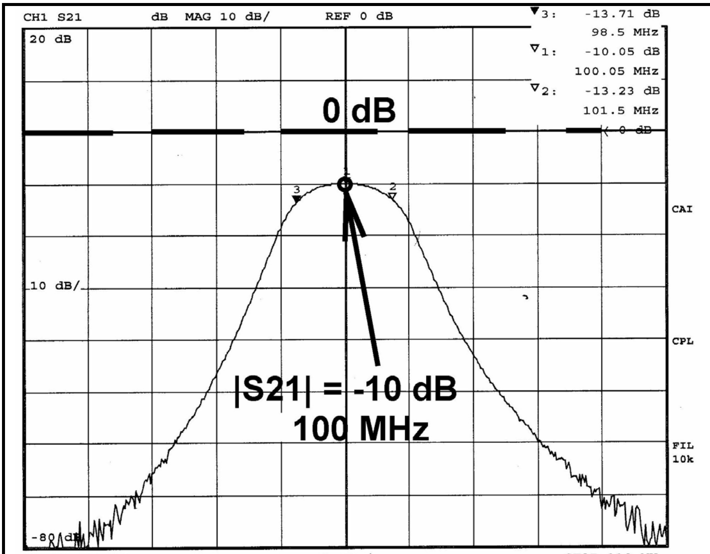


Fig 16: Transmission curve from 90 to 120MHz.

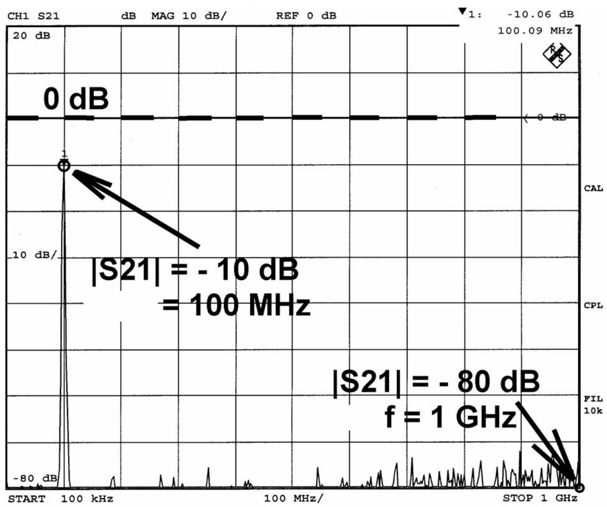


Fig 17: The stop band from 100KHz to 1GHz.

or Q = 72. But since not only the coils but also the capacitors play a part in these losses, it would be rewarding to do another experiment here using very expensive but high quality microwave ceramic capacitors (as incorporated used in the Satellite LNBs).

Finally, Fig. 17 shows the stop band in the range from 100kHz to 1GHz. In principle, no unpleasant surprises should be expected here as, through the use of several SMD capacitors in each resonant circuit, the inherent resonance is pushed sufficiently far upwards. To recap: the inherent inductance of these capacitors does not depend on the capacitance value but on the size of the housing, and for “0805” is about 0.5nH. If we use several capacitors in parallel the inductances is in parallel and there is a corresponding fall in the total inductance. So it is only above this inherent resonance that the filter attenuation collapses, because the resonant circuit no longer displays capacitive behaviour, being replaced by inductances. And unfortunately their reactive impedances then diminish as the frequency rises.

The reduction in the filter attenuation as the frequency rises can be prevented. Since we are dealing with a direct coupling of the output to the input the effects of these capacitors own inherent inductance, which we have just been discussing, also have a role to play here, we must use three capacitors in each resonant circuit, instead of just two.

One other comment: as a precaution, the inside of the cover was laminated with a conducting foamed material 2mm thick, in order to suppress the expected housing resonances in the GHz range. However, the effect of all these measures for the range exceeding 1GHz was not investigated further.

8. Summary and outlook

The combination of modern design and simulation software, including undesirable “parasitics”, together with a correct circuit board layout and correct housing construction, means that nowadays even a DIYer of limited means can assemble high quality circuits with precisely pre-

```
                FilDes--Filter Design System--Ver 1.20
                        Narrow BandPass Filter
What is the value for the inductors? (in nH)
72                           Resonating caps are:
Coupling caps are:           C(1) = 16.27 pF
C(1,2) = 0.461 pF            C(2) = 15.90 pF
C(2,3) = 0.369 pF            C(3) = 16.00 pF
C(3,4) = 0.369 pF            C(4) = 15.90 pF
C(4,5) = 0.461 pF            C(5) = 16.27 pF
The characteristic impedance of the filter is 2544.98 ohms
Match to a lower rs/rl? (Y/any key)
Default impedance is 50.00 ohms.  Type 'D' for different src and load
or hit any key to match to default.
Add 3.108 pf to the source end, and 3.108 pf to the load end.
Then change C(1) to 13.226 pf and C(5) to 13.226 pf.
(S)ave to file (P)rint or (C)ont?
_

   Type: NBP  Poles: 5  Ripple: 0.30  Zsrc 50.00 Fo 145.00 MHz
   BW design (ripple or 3 dB): 3 dB
```

Fig 18: A design for a 145MHz filter using "fds".

dictable characteristics. Converting to other frequencies is not a problem either, a pocket calculator and version 2.1 of PUFF are all you need!

In conclusion, I'd like to make a wish come true for a radio ham friend of mine: During a technical discussion on the problems arising in relation to the development of the bandpass filter, he said: “Now, do something aimed directly at radio amateurs. I could make good use of a filter like that if I could use your converter idea, but with a 2m receiver instead of the car radio”.

He's right, and so Fig. 18 shows just such a design. For this project, the circuit inductance has been reduced to 72nH (for the next smallest filter obtainable can be altered only between 76nH and 67nH) and the band width has been increased to 6MHz due to the higher mean frequency. The simulation in the range of 120 to 160MHz is shown in Fig. 19, where the work was carried out with Q = 100 (this shows the enormous values for the stop band at 120 or 160MHz!).

Complete development requires a little more work because the microstrip line in the centre of the board shows up parallel capacitances for each resonant circuits. True, these are only percentage changes, but this influence unfortunately does slowly make itself felt.

A series of such line sections with various lengths can be listed in PUFF list F3 and they can be introduced between the individual filter components in accordance with the board layout. Then, of course, comes the laborious precision work to correct the circuit capacitors.

Due to the higher operating frequency, the direct capacitive coupling between the input and output sockets within the housing can now have a greater effect on the filter attenuation and can make it worse. So presumably dividing walls are required and it looks as if this could mean a new, independent project.

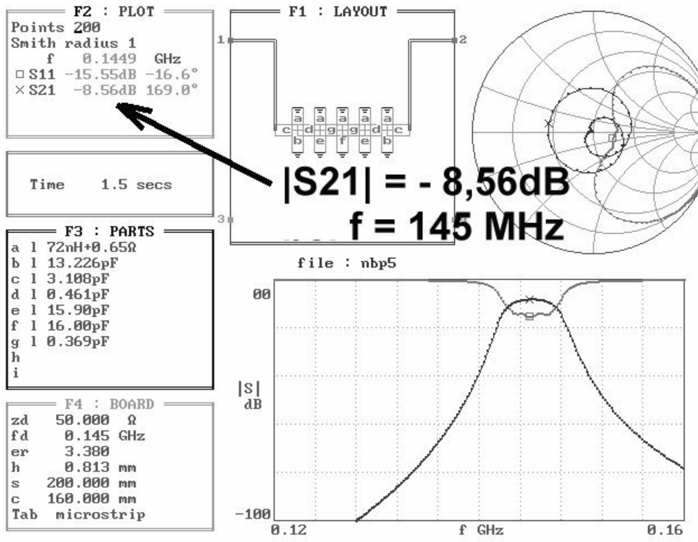


Fig 19: PUFF simulation of a 2m bandpass filter from 120 to 160MHz.

9. A disadvantage which unfortunately could not be avoided

Everything is working excellently, the filter is doing its duty, the articles written and now it has to be sent off. What is there left to do? Well, something does come creeping up now from an unexpected quarter. In this case from Finland - the CD with the newest test version 7.80 of APLAC turned up on my desk.

So you run the update and, just for interest, test the improvements, using the new version on existing completed projects. And what does this lead to? True, you can certainly calculate the inter-digital capacitor again, with its dimensions and fractional capacities, but generating the S parameter file (and thus the sweep) is barred, the reason given being "Memory restricted in this version". Following several emails and some overheating among the specialist brains working things out in Helsinki, this is the situation:

- The two tasks (i.e. S parameter sweep AND capacitor calculation) can function together only if you use version 7.51, which is indeed what the author has been using up to now.
- With the newer versions, only the capacitor calculations can be carried out since, due to the recently improved model, the simulation cost for sweeps has increased, and has therefore exceeded the limits of the student version.
- APLAC is rather embarrassed, and in such circumstances may well wish they'd been a bit less nit-picking in issuing cheap-rate "University and Education Licenses". So they are being very generous about issuing free 45 day test complete versions (and you can apply more than once....). But please contact APLAC direct with your queries!

The author can also suggest another solution, which is to carry on using the

previous version 7.51. His email address is: krausg@elektronikschule.de

10. Literature references

[1] Puff beginners project: Low-noise amplifier for the 137MHz NOAA weather satellite range or for the 145MHz 2m amateur radio band. Part 3, Section 12.2.: Building an inter-digital capacitor by Gunthard Kraus. UKW Berichte 3/1999, Page 170 (This article did not appear in VHF Communications but can be translated if there is sufficient demand - Andy)

[2] Design and building of microwave circuit .Part 10: Development of a 2GHz oscillator. Section 13.7.: Dimensioning of an inter-digital capacitor by Gunthard Kraus. UKW Bericte 2/1999, Page 117 (This article did not appear in VHF Communications but can be translated if there is sufficient demand - Andy)

[3] An Interesting Program APLAC by Gunthard Kraus. VHF Communications 2/2003, pp 90 - 105.

[4] Problem with running Puff on Window 98, Windows ME and Windows XP, and how to eliminate them by Gunthard Kraus. VHF Communications 4/2002, pp 229 - 231.

[5] Lets try again with PUFF by Gunthard Kraus. VHF Communications 3/2003, pp 170 - 180.